In the claims:

Please substitute the following full listing of claims for the claims as originally filed or most recently amended.

1. (Original) A fault analyzing system for finding candidates of plural kinds of fault, comprising:

a fault propagation path presuming unit presuming logic state along signal paths for determining fault propagation paths connected to output terminals where error signals are observed, and specifying fault terminals related to nodes on said fault propagation paths for producing pieces of related fault terminal information on plural time planes; and

a fault candidate weighting unit merging the pieces of related fault terminal information on one of said plural time planes with the pieces of related fault terminal information on another of said plural time planes in different manners so as to determine plural groups of fault candidates for said plural kinds of fault.

2. (Original) The fault analyzing system as set forth in claim 1, further includes

a data memory unit connected to said fault propagation path presuming unit and said fault candidate weighting unit, and storing first pieces of data information representative of a layout of an electric circuit to be analyzed, second pieces of data information representative of said logic state presumed by said fault propagation path presuming unit and logic state expected along said signal path and said pieces of related terminal information.

3. (Original) The fault analyzing system as set forth in claim 2, in which said fault propagation path presuming unit includes

a fault terminal searching means accessing said first pieces of data information and said second pieces of data information so as to search said data memory for said fault terminals,

a partial circuit extracting means accessing said first pieces of data information so as to extract partial circuits related to said fault terminals from said electric circuit,

an internal logic state presuming means accessing said first pieces of data information and said second pieces of data information so as to presume said fault propagation paths,

a logic state registration means for storing the second pieces of data information representative of said logic state along said fault propagation paths in said data memory, and

a related terminal registration means accessing said first pieces of data information and said second pieces of data information representative of said logic state along said fault propagation paths so as to specify said fault terminals related to said nodes on said fault propagation paths.

4. (Original) The fault analyzing system as set forth in claim 3, in which said related terminal registration means determines a relation between said nodes of said partial circuits and output terminals of said partial circuits and a relation between said output terminals of said partial circuits and said fault terminals related to logic circuits in said electric circuit so that said pieces of related terminal information are managed in a hierarchy in said data memory.

5. (Original) The fault analyzing system as set forth in claim 1, in which said fault candidate weighting unit includes plural weighting means merging said pieces of related fault terminal information on said

one of said plural time planes with said pieces of related fault terminal information on said another of said plural time planes in said different manners, respectively, so as to determine said plural groups of fault candidates for said plural kinds of fault, respectively.

6. (Original) The fault analyzing system as set forth in claim 5, in which one of said plural weighting means determines one of the group of stuck- up fault candidates, the group of open- fault candidates and the group of bridge- fault candidates.

7. (Original) The fault analyzing system as set forth in claim 6, in which another of said plural weighting means determines another of said group of stuck- up fault candidates, said group of open- fault candidates and said group of bridge- fault candidates.

8. (Original) The fault analyzing system as set forth in claim 7, in which yet another of said plural weighting means determines yet another of said group of stuck- up fault candidates, said group of open- fault candidates and said group of bridge- fault candidates.

9. (Original) The fault analyzing system as set forth in claim 2, in which said fault candidate weighting unit includes a weighting means having

a related fault terminal information searching means accessing said pieces of related terminal information so as to obtain said plural time planes, and

a related fault terminal information merging means merging said pieces of related fault terminal information on said one of said plural time planes with said pieces of related fault terminal information on said another of said plural time planes in so far as

said pieces of related fault terminal information on said one of said plural time planes are identical in logic state and location on said plural time planes with said pieces of related fault terminal information on aid another of said plural time planes, thereby determining a group of stuck- up fault candidates.

10. (Original) The fault analyzing system as set forth in claim 9, in which said one of said plural weighting means further includes a candidate sorting means for sorting said stuck- up fault candidates with the number of said fault terminals serving as a weight for making a list of said stuck- up fault candidates arranged in order of importance.

11. (Original) The fault analyzing system as set forth in claim 2, in which said fault candidate weighting unit includes a weighting means having

a related fault terminal information searching means accessing said pieces of related terminal information so as to obtain said plural time planes, and

a related fault terminal information merging means merging said pieces of related fault terminal information on said one of said plural time planes with said pieces of related fault terminal information on said another of said plural time planes in so far as said pieces of related fault terminal information on said one of said plural time planes are identical in location on said plural time planes with said pieces of related fault terminal information on said another of said plural time planes, thereby determining a group of open- fault candidates.

12. (Original) The fault analyzing system as set forth in claim 11, in which said one of said plural weighting means further includes a candidate sorting means for

sorting said open- fault candidates with the number of said fault terminals serving as a weight for making a list of said open- fault candidates arranged in order of importance.

13. (Original) The fault analyzing system as set forth in claim 9, in which said fault candidate weighting unit further includes another weighting means having

a related fault terminal information searching means accessing said pieces of related terminal information so as to obtain said plural time planes, and

a related fault terminal information merging means merging said pieces of related fault terminal information on one of said plural time planes with said pieces of related fault terminal information on another of said plural time planes in so far as said pieces of related fault terminal information on said one of said plural time planes are identical in location on said plural time planes with said pieces of related fault terminal information on said another of said plural time planes, thereby determining a group of open- fault candidates.

14. (Original) The fault analyzing system as set forth in claim 13, in which said another weighting means further includes a candidate sorting means for sorting said open- fault candidates with the number of said fault terminals serving as a weight for making a list of said open- fault candidates arranged in order of importance.

15. (Original) The fault analyzing system as set forth in claim 13, in which said fault candidate weighting unit further includes yet another weighting means having

a candidate selecting means selectively pairing said open- fault candidates for forming plural candidate pairs,

an unqualified candidate eliminating means checking the second pieces of data information representative of the expected logic state and said pieces of related fault terminal information to see whether or not each candidate pair meets the conditions of a bridge- fault, and eliminating said each candidate pair if said each candidate pair does not meet said conditions so as to determine qualified candidate pairs,

another related fault terminal information merging means merging said pieces of related fault terminal information related to said qualified candidate pairs on one of said plural time planes with said pieces of related fault terminal information related to said qualified candidate pairs on another of said plural time planes for determining a group of bridge- fault candidates.

16. (Original) The fault analyzing system as set forth in claim 15, in which said yet another weighting means further includes a candidate sorting means for sorting said bridge- fault candidates with the number of said fault terminals serving as a weight for making a list of said bridge- fault candidates arranged in order of importance.

17. (Original) The fault analyzing system as set forth in claim 15, in which one of said conditions is that the open- fault candidates of each pair have the same expected logic state on each time plane, and another of said conditions is that the fault terminals related to one of said open- fault candidates of each pair are contained in a group of the fault terminals related to the other of said open- fault candidates of

said pair on each time plane.

18. (Original) A method for finding candidates of plural kinds of fault, comprising the steps of:

a) determining output terminals where error signals are observed;

b) specifying fault terminals related to nodes of an electric circuit found on fault propagation paths connected to said output terminals for producing pieces of related fault terminal information on plural time planes; and

c) merging the pieces of related fault terminal information representative of the fault terminals related to the nodes on one of said plural time planes with the pieces of related fault terminal information representative of the fault terminals related to said nodes on another of said plural time planes in different manners so as to determine plural groups of fault candidates for said plural kinds of fault.

19. (Original) The method as set forth in claim 18, in which said step b) includes the sub-steps of

b-1) accessing first pieces of data information representative of a layout of said electric circuit and second pieces of data information representative of logic state in said electric circuit and expected logic state stored in a data memory so as to determine said fault terminals,

b-2) accessing said first pieces of data information stored in said data memory so as to extract partial circuits related to said fault terminals from said electric circuit, and

b-3) accessing said first pieces of data information and said second pieces of data information stored in said data memory so as to presume said fault propagation paths,

b-4) storing the second pieces of data information

representative of said logic state along said fault propagation paths in said data memory, and

b-5) accessing said first pieces of data information and said second pieces of data information representative of said logic state along said fault propagation paths so as to specify said fault terminals related to said nodes on said fault propagation paths.

20. (Original) The method as set forth in claim 18, in which said step c) includes the sub-steps of

c-1) determining plural groups of pieces of related fault terminal information associated with said plural time planes, respectively,

c-2) merging said pieces of related fault terminal information of one of said plural groups with said pieces of related fault terminal information of another of said plural groups in a first manner so as to make a first list of candidates for a first kind of fault, and

c-3) merging said pieces of related fault terminal information of one of said plural groups with said pieces of related fault terminal information of another of said plural groups in a second manner so as to make a second list of candidates for a second kind of fault.

21. (Currently Amended) The method as set forth in claim 20, in which said step c) further includes the sub-step of

c-4) merging said pieces of related fault terminal information of one of said plural groups with said pieces of related fault terminal information of ~~another~~ one of said plural groups with said pieces of related fault terminal information of another of said plural groups in a third manner so as to make a ~~first~~ third list of candidates for a third kind of fault.

22. (Original) The method as set forth in claim 20, in which said pieces of related fault terminal information

of said one of said plural groups are merged with said pieces of related fault terminal information of said another of said plural groups if each of said pieces of related fault terminal information is identical in logic state and location on the time planes with associated one of said pieces of related fault terminal information of said another of said plural groups for making said first list of candidates for a stuck- up fault in said step c-2).

23. (Original) The method as set forth in claim 20, in which said pieces of related fault terminal information of said one of said plural groups are merged with said pieces of related fault terminal information of said another of said plural groups if each of said pieces of related fault terminal information is identical in location on the time planes with associated one of said pieces of related fault terminal information of said another of said plural groups for making said second list of candidates for an open- fault in said step c-3).

24. (Original) The method as set forth in claim 21, in which said candidates on said second list are selectively paired with one another for forming plural candidate pairs on each time plane, and the pieces of related fault terminal information related to one of the candidates of each pair are merged with the pieces of related fault terminal information related to the other candidate of said each pair if each of said candidates of said each pair meet conditions of said third kind of fault.

25. (Original) The method as set forth in claim 24, in which one of said conditions is that said candidates of each pair have the same expected logic state on each time plane, and another of said conditions is that the

fault terminals related to one of said candidates of each pair are contained in a group of the fault terminals related to the other of said candidates of said pair on each time plane.

26. (Original) An information storage medium for storing a computer program representative of a method for finding candidates of plural kinds of fault, comprising the steps of:

a) determining output terminals where error signals are observed;

b) specifying fault terminals related to nodes of an electric circuit found on fault propagation paths connected to said output terminals for producing pieces of related fault terminal information on plural time planes; and

c) merging the pieces of related fault terminal information representative of the fault terminals related to the nodes on one of said plural time planes with the pieces of related fault terminal information representative of the fault terminal related to said nodes on another of said plural time planes in different manners so as to determine plural groups of fault candidates for said plural kinds of fault.

27. (Original) The information storage medium as set forth in claim 26, in which said step b) includes the sub-steps of

b-1) accessing first pieces of data information representative of a layout of said electric circuit and second pieces of data information representative of logic state in said electric circuit and expected logic state stored in a data memory so as to determine said fault terminals,

b-2) accessing said first pieces of data information stored in said data memory so as to extract partial circuits related to said fault terminals from

said electric circuit, and

b-3) accessing said first pieces of data information and said second pieces of data information stored in said data memory so as to presume said fault propagation paths,

b-4) storing the second pieces of data information representative of said logic state along said fault propagation paths in said data memory, and

b-5) accessing said first pieces of data information and said second pieces of data information representative of said logic state along said fault propagation paths so as to specify said fault terminals related to said nodes on said fault propagation paths.

28. (Original) The information storage medium as set forth in claim 26, in which said step c) includes the sub-steps of

c-1) determining plural groups of pieces of related fault terminal information associated with said plural time planes, respectively,

c-2) merging said pieces of related fault terminal information of one of said plural groups with said pieces of related fault terminal information of another of said plural groups in a first manner so as to make a first list of candidates for a first kind of fault, and

c-3) merging said pieces of related fault terminal information of one of said plural groups with said pieces of related fault terminal information of another of said plural groups in a second manner so as to make a second list of candidates for a second kind of fault.

29. (Original) The method as set forth in claim 28, in which said step c) further includes the sub-step of c-4) merging said pieces of related fault terminal information of one of said plural groups with said pieces of related fault terminal information of another of said plural groups in a third manner so as to make a

first list of candidates for a third kind of fault.

30. (Original) The method as set forth in claim 28, in which said pieces of related fault terminal information of said one of said plural groups are merged with said pieces of related fault terminal information of said another of said plural groups if each of said pieces of related fault terminal information is identical in logic state and location on the time planes with associated one of said pieces of related fault terminal information of said another of said plural groups for making said first list of candidates for a stuck- up fault in said step c-2).

31. (Original) The method as set forth in claim 28, in which said pieces of related fault terminal information of said one of said plural groups are merged with said pieces of related fault terminal information of said another of said plural groups if each of said pieces of related fault terminal information is identical in location on the time planes with associated one of said pieces of related fault terminal information of said another of said plural groups for making said second list of candidates for an open- fault in said step c-3).

32. (Original) The method as set forth in claim 29, in which said candidates on said second list are selectively paired with one another for forming plural candidate pairs on each time plane, and the pieces of related fault terminal information related to one of the candidates of each pair are merged with the pieces of related fault terminal information related to the other candidate of said each pair if each of said candidates of said each pair meet conditions of said third kind of fault.

33. (Original) The method as set forth in claim 32, in which one of said conditions is that said candidates of each pair have the same expected logic state on each time plane, and another of said conditions is that the fault terminals related to one of said candidates of each pair are contained in a group of the fault terminals related to the other of said candidates of said pair on each time plane.